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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/581,873	06/05/2006	Tim Niggemeier	PD030127	3929

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EXAMINER	
GIARDINO JR, MARK A	
ART UNIT	PAPER NUMBER
2185	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/581,873	NIGGEMEIER ET AL.	
	Examiner	Art Unit	
	MARK A. GIARDINO JR	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 December 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) _____ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

The Examiner acknowledges the applicant's submission of the amendment dated 12/19/2008. At this point claims 1 and 13 have been amended. Thus, claims 1-14 are pending in the instant application.

The instant application having Application No. 10/581,873 has a total of 14 claims pending in the application, there are 2 independent claims and 12 dependent claims, all of which are ready for examination by the examiner.

OBJECTIONS TO THE SPECIFICATION

The specification is objected to as failing to properly describe the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: the specification often recites "channels" performing active functions such as accessing (Page 7 Line 34 of the specification), accepting data (Page 7 Lines 35-36 of the specification), and sending commands (Column 10 Lines 10-16). While examples of channels are given on Page 7 of Applicant's specification as a CPU, this is not an explicit definition, and one of ordinary skill in the art would interpret a channel as a bus that holds data, which is a passive component of a computer system and is thus unable to access data, accept data, and send commands. Appropriate correction is required.

REJECTIONS NOT BASED ON PRIOR ART

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-14 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 1 and 13 recite the limitations "IC" and "DRAM", and it is unclear what these acronyms stand for. What the letters stand for must be explicitly stated at least once, after which an acronym may be used. Appropriate correction is required.

Claims 1 and 13 have no clear delineation between the preamble and the body of the claim, thus it is unclear how the limitations of the claim are to be interpreted. Appropriate correction is required.

Claims 1-12 and 14 recite a method claim, but the steps performed in the method are unclear and must be more clearly shown. Appropriate correction is required.

Claims 1 and 13 recites the limitation "the transmissions". There is insufficient antecedent basis for this limitation in the claim. Appropriate correction is required.

Claims 1 and 13 recite the limitation "and communicates with the IC" but it is unclear which device is doing the communicating. Appropriate correction is required.

Claim 4, 5, 13, and 14 recite the word "it". There is insufficient antecedent basis for this limitation in the claim, and what "it" refers to must be clearly stated. Appropriate correction is required.

Claim 1 recites the limitation "transmissions of memory bank commands of multiple channels". One of ordinary skill in the art would interpret a channel as a bus

that holds data, which is a passive component of a computer system and is thus unable to transmit data, rendering the claim unclear. Appropriate correction is required.

Claim 6 recites the limitation "the channels access physically separate memory areas". One of ordinary skill in the art would interpret a channel as a bus that holds data, which is a passive component of a computer system and is thus unable to access memory, rendering the claim unclear. Appropriate correction is required.

Claim 7 recites the limitation "the channels access jointly used memory areas in the external DRAM". One of ordinary skill in the art would interpret a channel as a bus that holds data, which is a passive component of a computer system and is thus unable to access memory, rendering the claim unclear. Appropriate correction is required.

REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 3, 4, 6, 7, 10, 13, and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mes (US 7,028,142) in view of Dowling (US 2002/0040429).

Regarding Claim 1, Mes teaches a method for communication between an IC **(processors 104)** and an external memory **(program memory 102 and arbitration logic 112)**, where the external memory has at least one memory bank **(Column 6 Lines 17-19, "a single bank is described in this example")** and communicates with the IC via two or more channels **(the multiple channels from the buffer to the arbitration logic in Figure 1A, thus each processor has its own channel)**, wherein transmissions of memory bank commands of multiple channels are prioritized on the basis of a static priority allocation for commands **("fetch accesses are preferably given a higher priority than prefetch/data accesses", Column 4 Lines 45-47, also in the last sentence of the abstract, thus fetch accesses are given a statically higher priority over prefetch/data accesses)** and the commands having the same static priority are further prioritized on the basis of a dynamic priority allocation for the channels **(the channels from the processors use a round-robin fetch arbiter, Column 4 Lines 23-32, thus the commands are given dynamic priority because of the round-robin arbiters 202 and 204 of Figure 2)**.

However, Mes does not explicitly teach the program memory as a DRAM. Dowling teaches using DRAM program memory **(**Paragraph 0039). It would have been obvious to a person having ordinary skill in the art at the time the invention was made to which the subject matter pertains to have used DRAM as the external memory in Mes because it is less expensive than many other types of memory, including SRAM.

Regarding Claim 3, Mes and Dowling teach all limitations of Claim 1, wherein the dynamic priority allocation for channels involves a channel being given the lowest

priority after a command has been sent (the round robin arbiter described in Column 4 Lines 23-32 of Mes moves a channel to lowest priority after a command has been sent).

Regarding Claim 4, Mes and Dowling meet all limitations of Claim 1, wherein the dynamic priority allocation involves one of the channels being given highest priority in the next clock cycle if it does not have the highest priority in the current clock cycle and another channel sends a command (the round robin arbiter described in Column 4 Lines 23-32 of Mes moves a channel to highest priority after a different channel sends a command).

Regarding Claim 6, Mes and Dowling meet all limitations of Claim 1, wherein the channels access physically separate memory areas in the external DRAM (Column 3 Lines 33-36, where an embodiment is shown to use several different memories and thus physically separate memory areas in the external DRAM).

Regarding Claim 7, Mes and Dowling teach all limitations of Claim 1, wherein the channels access jointly used memory areas in the external DRAM and the assurance is given that no successive access operations to a jointly used memory area will arise ("a single wide memory can be used", Column 3 Lines 31-32, thus the processors may use joint areas of memory and to ensure data integrity, successive access operations are obviously limited).

Regarding Claim 10, Mes and Dowling teaches all limitations of Claim 1, wherein two successive access operations to a memory bank are permitted when they are made to the same row in the memory bank (the memory is one bank, Column 6 Line

19-20, and the round robin and static allocation permit successive operations to the memory regardless of the row).

Claim 13 is the memory controller with the same limitations as Claim 1, and is rejected under similar rationale.

Claim 14 is the appliance for reading and/or writing to storage media with the same limitations of Claim 1, and is rejected under similar rationale.

Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mes and Dowling in view of Kuddes (US 5,418,920).

Mes and Dowling teach all limitations of Claim 1 as described above. However, Mes and Dowling do not specifically teach a channel losing the highest priority only when it can send a command. Kuddes teaches a round robin where a channel is moved to the bottom only if it uses the bus (Column 7 Line 65 to Column 8 Line 12). It would have been obvious to a person having ordinary skill in the art at the time the invention was made to which the subject matter pertains to have had a channel lose priority only when it can send a command because this ensures that a channel that has not used the bus recently is allowed access to the memory.

Claims 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mes and Dowling in view of Wheeler et al (US 6,983,350).

Mes and Dowling teaches all limitations of Claim 1 as described above. However, Mes and Dowling do not teach always having an access operation to another

memory bank affected between them. Wheeler teaches alternating memory banks (Column 5 Lines 33 to 42 in Wheeler, alternating between an even and odd memory bank places at least one access operation between each bank).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to which the subject matter pertains to arrange memory operations in such a way. Wheeler provides the motivation when he states that the bandwidth of the RAM is improved (Column 5 Lines 40-42 in Wheeler).

Claims 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mes and Dowling in view of Chen et al (US 2003/0051108).

Mes and Dowling teach all limitations of Claim 1 as described above. However, Mes and Dowling do not teach a network provided which allows at least one channel to access various memory banks. Chen teaches a network (Bank Usage Sorter 110 in Chen) that allows the channels to access any memory bank (paragraph 0014, also see Figure 3 in Chen). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to which the subject matter pertains to have used this network to distribute the memory data evenly across the banks because this reduces costs (see Paragraph 0015 in Chen).

Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mes and Dowling in view of LaBerge (US 2001/0044885).

Mes and Dowling teach all limitations of Claim 1 as described above. However, Mes is silent on the details of how the memory bank works. LaBerge teaches a memory bank that has a state machine (containing at least the states 'idle' and 'not idle', see Paragraph 0023 and Figure 8 in LaBerge). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to which the subject matter pertains to have used a state machine to control the memory banks because tracking idle states results in reducing latency incurred between successive memory operations (see Paragraph 0019 in LaBerge).

Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mes and Dowling in view of the power point entitled "Random Access Memory".

Mes and Dowling teaches all limitations of Claim 1 as described above. However, Dowling does not teach the composition of the DRAM memory. "Random Access Memory" teaches combining several RAM modules into a single RAM module and a chip enable signal (called chip select in the power point) to select the desired module (see Slides 17 and 18). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to which the subject matter pertains to have combined the RAM modules this way because it allows for larger memories to be made (see Slide 18 in "Random Access Memory").

ARGUMENTS CONCERNING PRIOR ART REJECTIONS

Rejections - USC 102/103

Applicant's arguments with respect to claims 1 and 13 that the static commands having the same static priority are then further prioritized due to dynamic priority has been considered and is persuasive. Thus, the prior rejections of Claims 1-14 have been withdrawn. However, new rejections have been made in view of newly found prior art references.

STATUS OF CLAIMS IN THE APPLICATION

The following is a summary of the treatment and status of all claims in the application as recommended by **M.P.E.P. ' 707.07(i)**:

CLAIMS REJECTED IN THE APPLICATION

Per the instant office action, claims 1-14 are subject of a first action non-final after RCE filed 12/19/2008.

DIRECTION OF FUTURE CORRESPONDENCES

Any inquiry concerning this communication or earlier communications from the examiner should be directed to M. Anthony Giardino whose telephone number is (571) 270-3565 and can normally be reached on Monday - Thursday 7:30am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Sanjiv Shah can be reached on (571) 272 - 4098. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

M.A. Giardino

/M.G./

Patent Examiner
Art Unit 2185

February 27, 2009

/Stephen Elmore/
Primary Examiner, Art Unit 2185